Investigation of Ripple Voltage Across Capacitor in Military CS101 Test by Using FFT-Based Time Domain Solution

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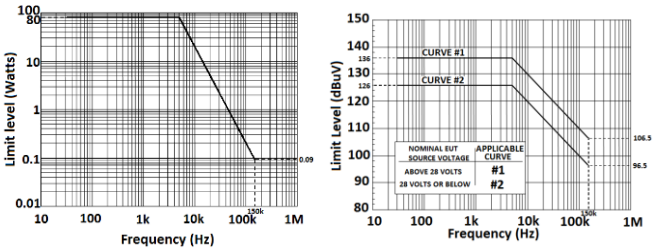
***Abstract*— The MIL-STD-461F CS101 test is one of the essential conducted immunity tests for military and aerospace equipment, however it includes some challenges in application. The major challenge is the necessity for the measurement of injected CS101 ripples under the power frequency of the EUT. The measurement of CS101 ripples on the power frequency is almost impossible without taking some extra precautions. In addition to the hard necessity of measuring the CS101 ripple voltage induced across the EUT power input, the other challenge of measuring the ripple voltage that drops across the 10 µF test capacitor under the AC power frequency of the EUT is now required by MIL-STD-461G, which aggravates the severe CS101 test conditions of AC devices. In this paper, we propose a FFT-based time domain solution and a method to instantly check the ripple voltage that drops across the power source side, in other words across the 10 µF test capacitor, during the test under the AC EUT power frequency and to verify that it is low enough and not affecting the reliability of the test. The method proposed in this paper significantly overcomes the CS101 test challenges and makes CS101 test results more accurate.**

Keywords*— *Aerospace, Capacitor, CS101, DFT, EMC, FFT, Immunity, Military, Susceptibility, Time Domain

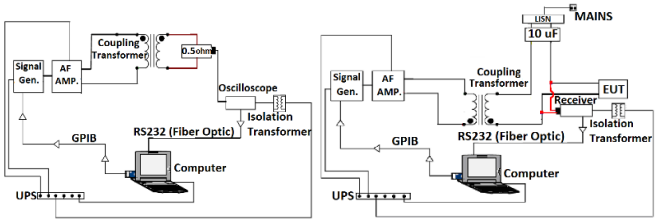
I. INTRODUCTION

The CS101 test defined in the standard MIL-STD461G [1] is applied to military and aerospace equipment by injecting low frequency sinusoidal voltage ripples to power ports of the Equipment Under Test (EUT) between 30 Hz - 150 kHz in order to determine susceptibility levels of the EUT. The CS101 test firstly requires a calibration process performed on a 0.5 Ω resistor. During the calibration, the power level seen on the Fig.1(a) is established on the 0.5 Ω resistor by means of an oscilloscope and an Audio Frequency (AF) coupling transformer as shown in the setup in Fig.2(a). In the test, the signal generator levels (or power) recorded in the calibration are applied to the EUT by using the same AF coupling transformer in accordance with the test setup shown in Fig.2(b). During the application, the voltage levels of CS101 ripples which are injected into the EUT must be continuously measured by an oscilloscope because the power level injected into the EUT or the ripple voltage level induced at the EUT power input, whichever reaches its limit first, limits and stops the leveling process. The voltage limit levels according to nominal source voltages of the EUT are given in Fig.1(b). The main challenge that arises during testing of AC equipment is the necessity for the detection of injected AC ripples due to the voltage limitation requirement of the standard. The measurement of CS101 ripples is strictly stipulated by the standard and vital for reproducible and reliable results with low uncertainty. In [2,3], we specially focused on the measurement methods of CS101 ripples under the power frequency and also on the comparison of the employed filters and their verifications.



(a) (b)

Fig.1. Calibration power limit and test voltage curves in CS101 [1], (a) CS101 calibration power curve, (b) CS101 test voltage curves



(a) (b)

Fig.2. CS101, (a) calibration setup, (b) test setup

In [3], we firstly proposed a method to verify filters and attenuators which are used for measuring CS101 ripples under the AC mains, thereafter applied this proposed verification method to two CS101 filters one of which had been designed by us. We also showed in [3] that the proposed verification method is not only used for verifying CS101 filters or attenuators, but also it can be employed to verify the entire CS101 test system from the filter to the test software screen.

In [4], we proposed a Fast Fourier Transform (FFT)-based time domain solution in order to easily separate CS101 ripples from the AC power frequency of the EUT by means of a simple oscilloscope and a piece of FFT-based software. We also demonstrated the advantages of the FFT-based solution over

the hardware filtering solutions in terms of higher accuracy and ease of use.

On top of the existing challenges of the CS101 test, the new version of the standard [1] requires verifying that the ripple voltage that drops on the power source side, namely across the 10 µF capacitor seen in Fig.2(b), is low enough and not affecting the reliability of the test results and not causing undertesting. This new addition creates a new challenge and also requires the measurement of the ripple voltage, which drops across the 10 µF capacitor, under the AC EUT power frequency in addition to the measurement of the ripple voltage at the EUT side. For that reason, in this paper, we specifically focus on the investigation and measurement of the ripple voltage that drops across the 10 µF capacitor in the time domain and on possible solutions to reduce this ripple voltage and route all the injected energy into the EUT. Finally, in order to accurately detect the ripple voltage that drops across the power source side and catch undertesting in advance as required by the standard, we propose a promising FFT-based time domain solution and a method using a simple oscilloscope, its two channels/probes and a special software solution without using cumbersome filter/attenuator solutions or special ripple detectors which require inclusion of insertion loss values, expensive and sensitive frequency selective receivers and time-consuming complex setup arrangements.

II. Induced Ripple Voltage Across Capacitor, FFT-Based Time Domain Solution And Experimental Setup

To be able to measure CS101 ripples injected into the EUT supplied by an AC power source and detect the ripple voltage that drops across the power source side, the power frequency must be cancelled and the great challenge of separation of CS101 ripples from the AC power frequency must be overcome. In this paper, we specially investigated the integration of a FFT-based time domain measurement method into the power source side of CS101 tests without using special filters or special ripple detectors in order to accurately measure the ripple voltage that drops across the 10 µF capacitor. We also developed a piece of effective software by using Visual C++ in order to apply the FFT-based time domain solution and precisely read CS101 ripples at the EUT power input and simultaneously on the 10 µF capacitor under the AC power frequency by means of a simple oscilloscope and its two 100:1 probes. One of the oscilloscope probes is connected to the EUT power input and the other is connected to the tips of the 10 µF capacitor. The designed software supports both the CS101 calibration and CS101 test phases. There is also a special checkbox on the software screen to activate the FFT-based time domain ripple measurement both across the 10 µF capacitor and across the power input of AC EUT. To verify the performance and effectiveness of the FFT-based time domain solution, in [4], we firstly performed a CS101 calibration on a 400 Ω resistor by using regular RMS readings without the FFT-based solution and without using an AC power source in the setup shown in Fig.3. Thereafter, we applied AC source voltage and frequency pairs given in Table 1 to the setup in turn without making any other change in the setup and performed tests by playing back the calibration power recorded in the calibration phase and using the FFT-based time domain solution. In this test phase, it is expected that the CS101 ripple voltage monitored via the FFT-based time domain solution is supposed to follow the voltage curve#1 seen in Fig.1(b) because we used the curve#1 in the calibration phase and the test setup was the same as the calibration setup except the presence of the AC power source and also we played back the calibration power in this test phase. As a result, in this stage of the research, the effectiveness and performance check of the FFT-based time domain solution was based on how good the ripple voltage monitored through the FFT-based time domain solution under the AC power frequency followed the calibration curve#1 across the 400 Ω resistor. For all the source voltage and frequency pairs stated in Table1, the FFT-based time domain solution perfectly achieved the accurate separation of CS101 ripples from the EUT power frequency and has been successfully validated [4].

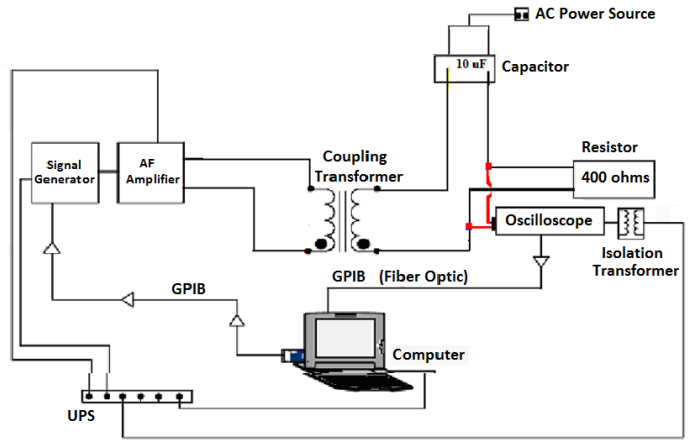


Fig.3. Validation setup for FFT-based time domain solution [4]

After the validation of the accurate measurement capability of the time-domain solution under all the checked source voltage & frequency pairs, we started to investigate the ripple voltage that drops across the 10 µF capacitor, in other words across the power source side. Firstly, during the CS101 test, per frequency and per leveling step, we acquired the scope data at the EUT power input by using the "channel1" of the oscilloscope and also simultaneously across the 10 µF capacitor by using the "channel2" of the oscilloscope through the developed software and then processed the data by using FFT-based algorithms in the same software to obtain power spectrum estimates, known as periodograms. MIL-STD461G states that below 10 kHz there is a possibility that a portion of the injected signal will drop across the power source rather than the test sample power input. Therefore, below 10 kHz when the specification limit potential cannot be developed across the test sample power input and the precalibrated power limit has been reached, it is incumbent on the tester to check that the missing signal level is not being dropped across the power source. If the missing potential is there (usually due to high impedance test facility EMI filters), then steps should be taken to lower the source impedance. This can be done on DC power by using a larger capacitor (~10 mF) in parallel with the 10 µF capacitor. With AC power that isn't possible and the best approach is to bypass facility EMI filters entirely, bringing unfiltered power into the room [1]. To investigate the ripple voltage that drops across the power source side, we

installed the setup shown in Fig.4 by using a variety of EUT samples.

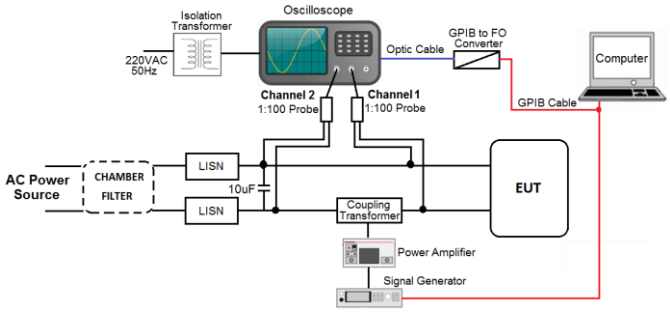


Fig.4. Setup of FFT-based time domain solution to measure the CS101 ripple voltage that drops across the 10 µF capacitor and also across the EUT power input under AC EUT power frequency

As seen in Fig.4, the first channel of the oscilloscope is connected across the EUT power input; the second channel is connected across the 10 µF capacitor. It should be specially noted here that the oscilloscope was supplied through an isolation transformer and the GPIB communication connection was provided by fiber optic cables to avoid any undesired ground connection. Also the ground tips of the two probes must be electrically connected to the same point as shown in Fig.4. The software solution developed by us performs smart activation of the FFT-based time measurement of the ripple voltage that drops across the 10 µF capacitor. It does not activate the measurement on the 10 µF capacitor as long as the voltage limit is reached and the test power is below the power limit (calibration power) during testing. If the test power reaches the calibration power and the CS101 power value starts to limit the leveling which means that the ripple voltage induced across the EUT power input is less than the curve#1 shown in Fig.1(b), the software activates the FFT-based time domain solution also for the measurement of the capacitor voltage in order to verify that the ripple voltage across the capacitor is low enough and the missing voltage of the EUT power input is not there. On the other hand, especially for this research, we activated the FFT-based time domain solution for the entire CS101 frequency range regardless of the voltage or power limiting in order to observe the ripple voltage induced across the EUT power input and across the 10 µF capacitor simultaneously in the entire frequency range.

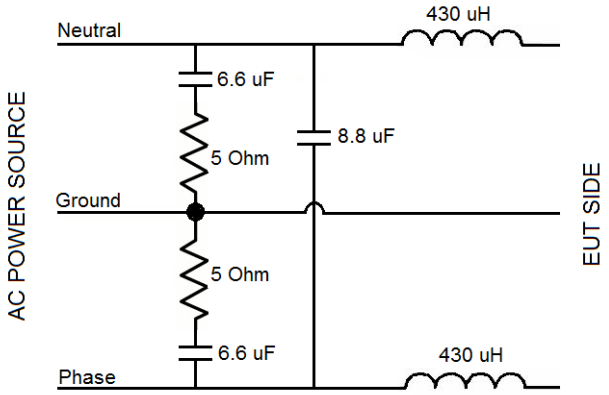


Fig.5. Chamber filter constructed and used at the power source side

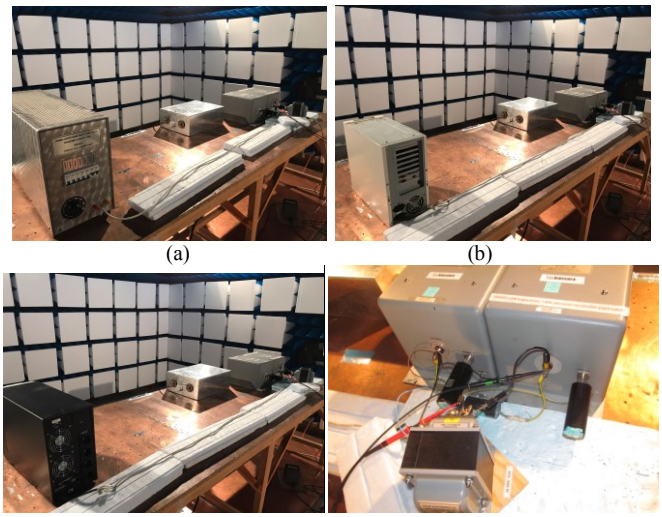


Fig.6. Test setup photos (a) Load, (b) PC, (c) UPS, (d) LISN side close-up

We performed CS101 tests in the test conditions stated in Table 2 in turn. As a chamber filter to be used at the power source side at the back of the Line Impedance Stabilization Networks (LISN), we constructed a chamber filter whose circuit is shown in Fig.5 and employed this developed filter in the research because the inclusion and removal of the actual commercial room filters installed on the external wall of our screened chamber were not an easy task. As seen in Table 2, we performed CS101 testing and measured the ripple voltage induced across the EUT power input and across the 10 µF capacitor under a variety of test conditions. We used a commercial power source (Manufacturer:Schaffner, Model:NSG1007, 45 kVA) along with 3 different EUT types. The first EUT was a regular load shown in Fig.6(a) which draws 8 A under 110 VAC, 60 Hz. The second EUT was a simple desktop Personal Computer (PC) shown in Fig.6(b). The third EUT was an Uninterruptible Power Source (UPS) shown in Fig.6(c). Each EUT was tested with and without the chamber filter in turn to observe the effects of the chamber filter on the test results and on the ripple voltage that drops across the 10 µF capacitor of the test setup. The close-up of the LISNs and the coupling transformer is given in Fig.6(d). After the first set of measurements, we also added an extra capacitor to the back of the LISNs at the power source side for the EUT type "load" in order to attempt to reduce the impedance of the power source side and subsequently lower the ripple voltage induced across the 10 µF capacitor of the test setup.

Table 1. AC power source voltage and frequency pairs applied to test setup to verify the time domain solution [4]

	Voltage (VAC)	**Frequency (Hz)**
Power Source 1	220	50
Power Source 2	115	400
Power Source 3	440	50
Power Source 4	190	60

Table 2. Test conditions used to investigate the ripple voltage induced across the 10 µF capacitor

Test Number	EUT Type	Power Source Voltage / Frequency	Chamber Filter	Additional Component
1	Load	110 VAC / 60 Hz	Yes	No
2	Load	110 VAC / 60 Hz	No	No
3	Load	110 VAC / 60 Hz	No	Extra 10 µF at the power source side
4	PC	220 VAC / 50 Hz	Yes	No
5	PC	220 VAC / 50 Hz	No	No
6	UPS	220 VAC / 50 Hz	Yes	No
7	UPS	220 VAC / 50 Hz	No	No

Tablo 3. FFT-based time domain measurement parameters

Frequency Range	100 Hz – 150 kHz
Sampling Frequency (f_s)	400 kSamples/s
FFT bin bandwidth (B_{bin})	10 Hz
FFT length (N_p)	40000
Number of segments per sample block (M)	1
Number of Blocks	1
Samples between segments (L)	Not applicable in our research as M is 1
Overlap Factor	Not applicable in our research as M is 1

As stated earlier, we employed periodogram estimation in the research to detect CS101 ripple signals on the AC power frequency. The periodogram estimate of the power spectrum associated with a finite length sequence of data samples, denoted by x[n], where n is the sample index, is expressed mathematically as

$$\mathrm{P}(\underline{\omega}) = \frac{1}{\mathrm{N_p}}\left|\sum_{\mathrm{n=0}}^{\mathrm{N_P-1}} \mathrm{x[n]e^{-jn\underline{\omega}}}\right|^2 \quad (1)$$

where N_P is the number of points, or samples, over which the periodogram is calculated, and ω is the normalised digital frequency given by

$$\underline{\omega} = \frac{2\pi \mathrm{f}}{\mathrm{f_s}} \quad (2)$$

where f_s is the sampling frequency, and f is the analogue frequency of interest [5]. In (1), the summation is recognised as the Discrete Fourier Transform (DFT) of the sampled data sequence. The |·| operator denotes taking the magnitude of the complex spectrum as produced by the DFT. The computationally efficient equivalent of the DFT is the FFT. It is necessary to square the magnitude response of the FFT in order to obtain a power spectrum. When measuring noise sources, the power spectrum measured using the periodogram varies with time. Bartlett [6] modified the periodogram so as to average the results over a number of power spectra or segments (M), hence reducing the variance of the measurements. The Bartlett periodogram is expressed mathematically as

$$P_B(\underline{\omega}) = \frac{1}{\mathrm{MN_p}}\sum_{\mathrm{m=0}}^{\mathrm{M-1}}\left|\sum_{\mathrm{n=0}}^{\mathrm{N_P-1}} \mathrm{x[mN_p + n]e^{-jn\underline{\omega}}}\right|^2 \quad (3)$$

The Fourier transform assumes that the signal being analyzed is continuous in time, but as the DFT operates over a finite time interval, and then a windowing function should be applied to the DFT to prevent spectral leakage. Spectral leakage is the result of discontinuities in the signal at the boundaries of the sample block due to truncation. In the Bartlett method, the sample blocks or segments that are used to calculate the periodogram are contiguous and non-overlapping. If a windowing function is applied to each sample block, the Bartlett periodogram could lead to loss of spectral information. Impulses that are close to the boundaries of the windows are attenuated more than impulses in the centre of the window. If the attenuated impulses have spectral content that is different from the non-attenuated impulses, then the spectral content of the attenuated impulses will be attenuated or lost. To reduce the attenuation or loss of spectral data on the boundaries of the windowed segment, the spectra can be averaged over several overlapping segments [5]. This leads to the Welch periodogram [7], which is given by

$$P_W(\underline{\omega}) = \frac{1}{\mathrm{MN_pR}}\sum_{\mathrm{m=0}}^{\mathrm{M-1}}\left|\sum_{\mathrm{n=0}}^{\mathrm{N_P-1}} \mathrm{x[mL + n]w[n]e^{-jn\underline{\omega}}}\right|^2 \quad (4)$$

where L is number of samples to skip from segment to segment and R is the window coherent gain factor. For overlapping sample blocks L must be in the range $0 < L < N_P$. It is typical to use an overlap factor of approximately 50%. The window coherent gain factor, R, is used to compensate for the gain of the window function w[n] and is given [5] by

$$\mathrm{R} = \sum_{\mathrm{n=0}}^{\mathrm{N_P-1}} \mathrm{w[n]} \quad (5)$$

In our research, we employed the hanning function given in (6) as a windowing function.

$$w[n] = 0.5\left(1 - cos\left(\frac{2\pi n}{\mathrm{N_P}}\right)\right) \quad (6)$$

For all of the FFT-based time domain measurements made in this research, the sampling frequency (f_s) used was 400 kSamples/s. The number of points in the FFT (N_P) was chosen to obtain approximately a 10 Hz resolution bandwidth whose calculation is given by (7). All the FFT-based measurement parameters used in the research are listed in Table 3.

$$B_{bin} = \frac{f_s}{N_p} \quad (7)$$

Where f_s is the sampling frequency and N_P is the number of samples (FFT length) [5].

Finally, the CS101 ripple voltage is calculated by using the output (P_W) of the Welch function per frequency as follows;

$$V(dB\mu V) = 20 * log10\left(2 * 1000000 * \sqrt{P_W}\right) \quad (8)$$

This final result yields the CS101 ripple voltage induced across the EUT power input for the oscilloscope channel 1 and across the 10 µF capacitor for the oscilloscope channel 2.

III. Experimental Results and Discussions

The FFT-based time domain verification results obtained in [4] without using any filters/attenuators (or any special ripple detectors) are given in Fig.7 for the AC power source voltage and frequency pairs presented in Table1. As shown in Fig.7, the ripple voltage levels were precisely and perfectly detected on the AC power source frequency by means of the FFT-based time domain solution even if the power source voltage was increased to 440 VAC that is the highest power source voltage in practice. When we study Fig.7 more carefully, we see that the maximum deviation from the expected curve is lower than 1 dB for most of the frequency range and it is less than 3 dB in the rest for all the checked power source voltage and frequency pairs, which verifies the good performance of the FFT-based solution.

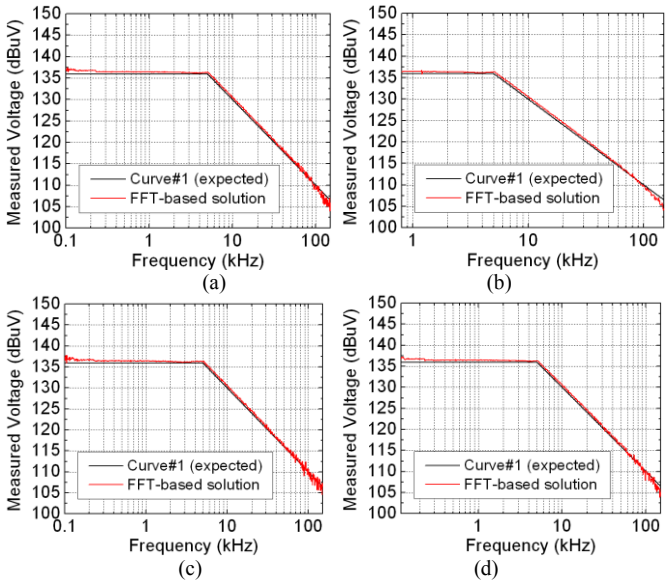


Fig.7. FFT-based time domain verification results (a) 220 VAC, 50 Hz, (b) 115 VAC, 400 Hz, (c) 440 VAC, 50 Hz, (d) 190 VAC, 60 Hz [4]

After the validation results, the measurement results of the ripple voltage which drops across the 10 µF test capacitor and which is detected by the FFT-based time domain solution under the AC power source frequencies are given between Fig.8 and Fig.10. As seen in Fig.8(a) for the first EUT type which is the regular load, with the chamber filter connected to the back of the LISN at the power source side, while the voltage limit curve#1 is reached in most of the frequency range, there is one region around 1 kHz where the ripple voltage induced across the EUT power input significantly goes below the curve#1 and the pre-calibrated power limit is reached. In this region, the ripple voltage that drops across the 10 µF capacitor markedly increases, which is clearly undertesting and means that missing potential is in fact dropped across the 10 µF capacitor, namely across the power source side, instead of the EUT due to the high impedance of the power source side.

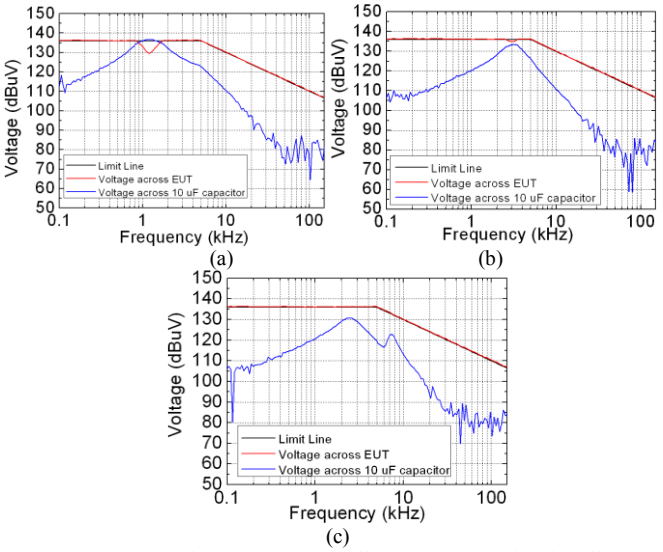


Fig.8. Results of load (a) with chamber filter, (b) without chamber filter, (c) extra 10 µF capacitor at the power source side

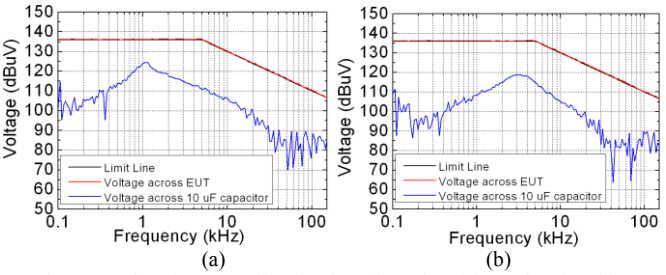


Fig.9. Results of PC (a) with chamber filter, (b) without chamber filter

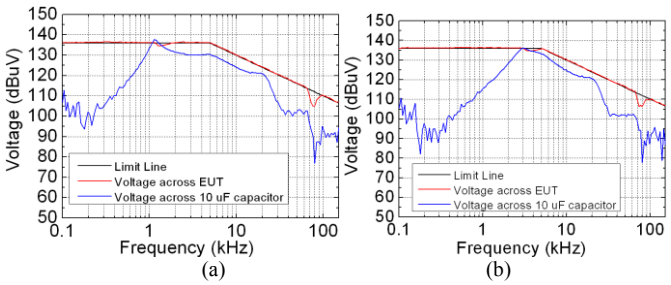


Fig.10. Results of UPS (a) with chamber filter, (b) without chamber filter

In this example, further action is required to reduce the ripple voltage that drops across the 10 µF capacitor and to avoid undertesting. When the chamber filter is removed from the setup as a first precaution, we see in Fig.8(b) that the removal of the chamber filter remarkably improves the situation and the ripple voltage that drops across the 10 µF capacitor is reduced and the ripple voltage injected into the EUT increases so that undertesting is partly removed. In this new case, the problematic frequency region is also slightly shifted to the 3 kHz region by the removal of the chamber filter. As another attempt at completely removing the undertesting, we put an extra 10 µF capacitor at the power source side at the back of

LISNs to reduce the impedance of the power source side. After the placement of the extra capacitor on the power source side, the problematic region seen in Fig.8(b) is completely rectified as seen in Fig.8(c) by this solution attempt and the ripple voltage that drops across the 10 µF capacitor decreases more. When we look at the results of the desktop computer in Fig.9, we see that the voltage limiting is activated in the full frequency range and the power limit obtained in the calibration is not reached at any frequency. Also as seen in Fig.9, the ripple voltage that drops on the 10 µF capacitor is not reaching a significant level in both the absence and presence of the chamber filter. In this PC example, there is no need to take further action to reduce the ripple voltage on the 10 µF capacitor as the voltage target across the EUT power input is accomplished in the full frequency range. Finally the results of the UPS are given in Fig.10. At first glance in Fig.10, we can expressly say that the removal of the chamber filter does not change the curves remarkably and only causes a slight frequency shift. In both of the graphs, the first frequency region around 1 kHz has slight undertesting (around 1 dB below the limit) due to the high ripple voltage that drops across the 10 µF capacitor but this slight undertesting can be neglected. On the other hand, the second frequency region around 100 kHz where the ripple voltage induced across the EUT power input is reduced below the curve#1 is more interesting and worth studying more carefully. In this frequency region around 100 kHz, while the ripple voltage induced across the EUT power input decreases, the ripple voltage across the 10 µF capacitor is not increasing significantly even decreasing in this range. For that reason, it is obvious that the missing potential is not across the 10 µF capacitor and the reduction in the potential across the EUT power input does not result from the power source side impedance. Consequently, as it seems that this reduction in the potential across the EUT power input is intrinsic to the EUT or its own cables, there is no undertesting here caused by the power source side and there is no need to take further action to reduce the power source side impedance. All the results also reveal that generally removal of chamber filters may be effective in lowering the power source side impedance and eliminating undertesting but sometimes this removal may not be effective contrary to expectations.

As a result, the proposed method in this paper significantly simplifies the achievement of the capacitor voltage measurement requirement of the new military standard; MILSTD461G under any AC EUT source voltage & frequency pair without using cumbersome filter/attenuator solutions. The filter/attenuator solutions usually require time-consuming and exhausting specific setup arrangements and need very sensitive and expensive frequency selective receivers that are normally not suitable to be used together with such high and risky power source voltage levels. Conversely, the proposed FFT-based time domain method does not require any expensive and sensitive frequency selective receivers such as spectrum analyzers and EMI receivers. Any simple digital oscilloscope with at least two channels along with its two 10:1 or 100:1 probes can be easily employed with the developed software solution that calculates the periodogram in order to measure the ripple voltage which drops across the 10 µF capacitor and across the EUT power input. With the introduced method and software, the ripple voltage induced across the 10 µF capacitor can be observed instantly during testing and undertesting can be detected in advance. Only one disadvantage can be mentioned for the proposed method as follows; as the software has to calculate the periodogram for each leveling step per frequency while reaching the target voltage level under AC EUT power frequency, this slightly slows down the CS101 test in comparison to the direct RMS reading from an oscilloscope or a spectrum analyzer.

CONCLUSION

In this paper, we introduced a measurement setup and a FFT-based time domain method to be able measure the ripple voltage that drops across the 10 µF of a CS101 setup under the AC power source frequency which is one of the prominent challenges of the latest military standard in addition to the existing challenge of reading the ripple voltage induced across the EUT power input. The proposed FFT-based time domain solution is very useful to easily and precisely separate the CS101 ripples, which are induced at both the power source side and the EUT side, from the AC power source frequency and to properly overcome the two challenging requirements of the standard without using cumbersome filter/attenuator solutions or complex setup arrangements.

ACKNOWLEDGMENT

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